REMARK

1.Rejection of claims 1-8 under 35 U.S.C. 103(a):

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,226,057).

Response:

Claim 1 is currently amended to overcome this rejection. In the amended claim 1, features in the "wherein" paragraph are moved to the "body" paragraph to make the feature more clear. No new matter is introduced. The amended claim 1 of the present application is repeated below for reference:

Claim 1: A liquid crystal display comprising:
a plurality of signal lines;
a plurality of scanning lines electrically connected to a scanning line control circuit; and
a plurality of pixels, each pixel comprising:
a liquid crystal cell having a pixel electrode and a storage capacitor, and
a switching transistor comprising a gate electrode connected to a scanning line, a drain electrode connected to one of the signal lines, and a source electrode connected to the pixel electrode, the gate electrode and the source electrode having an overlapping region, the size of the overlapping region of a pixel closer to the scanning line control circuit being smaller than the size of the overlapping region of another pixel farther from the scanning line

control circuit.

Lee discloses a dielectric film structure arranged in pairs. As shown in FIG. 4 of Lee's disclosure, by extending pixel electrodes 26n, 26n+1, 26n+2 of each unit cell to a given position of surface of the corresponding gate line 14m, third capacitors are secured, which is formed by a combination of the pixel electrodes 26n, 26n+1, 26n+2, the corresponding gate line 14m, and insulator interposed therebetween. In this case, since the first pixel electrode 26n+1 in even column Cn+1 is placed at the lower level layer, e.g., on the first dielectric film, between the first pixel electrode 26n+1 and the gate line 14m corresponding to the first pixel electrode 26n+1, the first dielectric film is only interposed, while since the second pixel electrodes 26n, 26n+2 in odd columns Cn, Cn+2 are placed at the upper level layer, e.g., on the second dielectric film, between the second pixel electrodes 26n, 26n+2 and the underlying corresponding gate line 14m, both layers of the first and second dielectric films are interposed. The dielectric film of odd columns (Cn, Cn+2) is thicker than that of even columns (Cn+1, Cn+3), so the capacitance of odd columns is smaller than that of even columns and needs compensation. So as to compensate the difference in capacitance, it is desirable to make larger the overlapped area between the pixel electrode 26n, 26n+2 in the odd columns Cn, Cn+2 and the gate bus line (col. 6, lines 1-38).

As mentioned above, Lee forms a thicker dielectric

film in the odd columns than in the even columns, so he has to make larger overlapped area in the odd columns than in the even columns to compensate the capacitance difference resulted from the different thickness of the dielectric film. However, Lee never teaches the concept of determining the size of the overlapping region between the gate electrode and the source electrode according to the distance between the pixel and the scanning line control circuit. That is, Lee fails to disclose "a liquid crystal display comprising the size of the overlapping region of a pixel closer to the scanning line control circuit being smaller than the size of the overlapping region of another pixel farther from the scanning line control circuit.", as is disclosed in the amended claim 1 of the present application. Therefore, Lee cannot achieve the advantages of adjusting the capacitance between the gate electrode and the source electrode to equal feed-through voltages of all pixels and prevent flicker in a TFT-LCD, as are provided by the present application.

The Examiner indicates that Lee does not explicitly suggest the area becomes larger as pixels are further away from the signal line, and believes that one ordinary skill in the art would contemplate adjusting the size of the overlapping area to provide desired effects. However, according to the legal concept of prima facie obviousness set forth in MPEP §2142, which states that,

"The teaching or suggestion to make the claimed

combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) see MPEP §2143 - §2143.03 for decisions pertinent to each of these criteria."

Since Lee never suggests the concept of determining the size of the overlapping region between the gate electrode and the source electrode according to the distance between the pixel and the scanning line control circuit, as is disclosed in the amended claim 1 of the present application, the Applicants respectfully believe that it is not obvious for one of ordinary skill in the art to contemplate Lee's disclosure to accomplish the present invention. Reconsideration of the amended claim 1 is politely requested.

The other independent claim 5 is also amended to include similar features as in the amended claim 1 and should be allowed for the allowance of independent claim 1 because Lee does not teach or suggest "the size of the first overlapping region being greater than the size of the second overlapping region" and "the size of the second overlapping region being greater than the size of the third overlapping region." as recited in independent claim 5. Thus, reconsideration of the amended claim 5 is politely requested.

As claims 2-4 and 6-8 are dependent upon the amended claims 1 and 5, they should be allowed at least because their base claims are allowed, as well as for the

reasons stated above. Reconsideration of claims 2-4 and 6-8 is therefore politely requested.

Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

Sincerely yours,

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